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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,772	09/12/2003	Makoto Shizukuishi	107317-00061	5771

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EXAMINER

LIVEDALEN, BRIAN J

ART UNIT	PAPER NUMBER
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2878

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/660,772

Applicant(s)

SHIZUKUISHI, MAKOTO

Examiner

Brian J. Livedalen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

This action is in response to amendment filed 11/28/05. Claims 1-20 are pending.

#### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation "an optical window formed on said first region and made of transparent material" is not sufficiently disclosed in the application. The specification in accordance with fig 3A shows an opening placed above the first region but not formed on it nor does the specification disclose that the opening is transparent.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-11, and 13-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakai (6784933).

In regard to claims 1, 7, and 11, Nakai discloses (fig. 1) a solid state image pickup device having a semiconductor substrate having a first layer of a first conductivity type (11); a second layer of a second conductivity type opposite to the first conductivity type (12), the second layer being formed on the first conductivity type layer of the semiconductor substrate; a first region (17) of the first conductivity type formed in the second layer and constituting a photodiode with the second layer; a first gate structure including a charge storage region (14) and a control gate (16), the first gate structure being formed on a surface of the semiconductor substrate adjacent to a portion of the first region, and the charge storage region being electrically isolated (13) from the first region; a second region of the first conductivity type (17) formed adjacent to the first gate structure on a side opposite to the first region, and constituting a non-volatile memory element with the first region and the first gate structure (column 5, lines 7-20); an optical window (fig. 7, 26) formed on the first region and made of transparent material (column 9, lines 3-6); and a control circuit for applying a first write voltage to the control gate of the first gate structure, the first write voltage being a write voltage for tunneling and injecting charges accumulated in the first region into the charge storage region (column 6, lines 55-68, column 10, line 63 – column 11, line 29); a second gate

structure (16a) of an insulated gate type (13a) formed adjacent to another portion of the first region; and a third region of the first conductivity type (18) formed adjacent to the second gate structure on a side opposite to the first region, the third region constituting an insulated gate type transistor with the first region and the second gate structure (column 5, lines 21-42); and a control circuit for applying a forward bias voltage to the first layer of the semiconductor substrate to supply current to the non-volatile memory element (column 9, lines 12-57).

In regard to claims 2 and 3, Nakai further discloses that the control circuit applies a second write voltage to the control gate of the first gate structure and to the second region after the first write voltage is applied, the second write voltage being a write voltage for injecting charges accumulated in the first region into the charge storage area region as hot carrier injection (column 3, line 67 – column 4, line 12); and a second gate structure (16a) of an insulated gate type (13a) formed adjacent to another portion of the first region; and a third region of the first conductivity type (18) formed adjacent to the second gate structure on a side opposite to the first region, the third region constituting an insulated gate type transistor with the first region and the second gate structure (column 5, lines 21-42).

In regard to claims 5, 9, and 13 Nakai discloses the charge storage region of the non-volatile memory element has a floating gate (column 5, lines 7-20).

In regard to claims 6, 10, and 14 Nakai discloses the charge storage region has an interface between a silicon nitride film and a silicon oxide film (column 12, lines 21-31).

In regard to claim 8, Nakai discloses having a control circuit for applying a bias voltage to the second gate structure to turn on the insulated gate type transistor for supplying current to the non-volatile memory element (column 4, lines 1-13).

In regard to claim 15, Nakai discloses (fig. 1) a driving method for a solid state image pickup device having the steps of: applying light to photodiodes distributed in a matrix layout and accumulating charges representative of image information (column 2, lines 49-67), the photodiodes being formed in a second layer (12) having a second conductivity type and being formed on a first layer (11) of a semiconductor substrate, the first layer having a first conductivity type opposite to the second conductivity type, the solid state image pickup device having optical windows (fig. 7, 25) made of transparent material and formed respectively on the photodiodes (column 9, lines 3-6); applying a first write control voltage to a control gate (16) of a non-volatile memory element having a charge storage region (14), the control gate and a drain region (17), the nonvolatile memory element being formed adjacent to each of the photodiodes, each of the charge storage regions being electrically isolated from associated one of the photodiodes, and tunneling and injecting at least a portion of the charges representative of the image information into the charge storage region as signal charges (column 6, lines 55-68) and applying a read control voltage to the non-volatile memory element to detect a threshold voltage corresponding to an amount of the signal charges injected into the charge storage region column 10, line 63 – column 11, line 29).

In regard to claims 16 -18, Nakai discloses an intermediate step before the reading step that applies a second write control voltage to the control gate and drain

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region of the non-volatile memory element and injecting as hot carriers at least a portion of the charges representative of the image information into the charge storage region as signal charges (column 3, line 67 – column 4, line 12); and a control circuit for applying a bias voltage to the second gate structure to turn on the insulated gate type transistor for supplying current to the non-volatile memory element (column 4, lines 1-13); and a control circuit for applying a forward bias voltage to the first layer of the semiconductor substrate to supply current to the non-volatile memory element (column 9, lines 12-57).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 12, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai (6784933) as applied to claim 1, 11, and 15 above, and further in view of Chi et al (6060742).

In regard to claims 4, 12, and 19, Nakai in view of Chi discloses an image pickup device with a control circuit. Nakai in view of Chi is silent regarding a third region of the first conductivity type projecting from an upper surface of the first conductivity type layer of the semiconductor substrate into the second conductivity layer. Chi et al. discloses (fig. 6) a region of the first conductivity type projecting from an upper surface of the first conductivity type layer of the semiconductor substrate into the second conductivity layer

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(603) and providing a forward bias to the layer of the substrate to supply a channel current (column 5, lines 8-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the third region of Chi et al. to the image pickup device of Nakai in order to provide a channel between the drain and the source and a resulting higher electron injecting efficiency.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai (6784933) as applied to claim 15 above, and further in view of Chi (US 6501109).

In regard to claim 20, Nakai discloses a imager driving method as disclosed above. Nakai remains silent regarding applying a reverse bias voltage to the first conductivity type layer of the semiconductor to drain charges accumulated beforehand in the photodiodes to a semiconductor substrate. However, discloses a method using a control circuit, which can apply a reverse voltage to the substrate to drain charges on the photodiode to the substrate (column 4, lines 40-45). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a step to drain the photodiodes in order to be able to detect more images.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

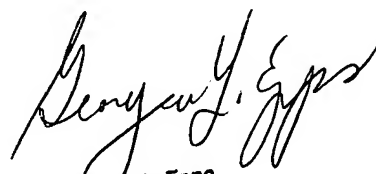
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Livedalen whose telephone number is (571) 272-2715. The examiner can normally be reached on 8:30 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Georgia Epps can be reached on (571) 272-2328. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bjl

  
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